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List of Abbreviations

BEOL	Back end of line
CG	Conversion gain
CS	Common source
GaAs	Gallium-Arsenide
HPA	High-power amplifier
InGaAs	Indium-Gallium-Arsenide
LNA	Low-noise amplifier
mHEMT	Metamorphic high-electron-mobility transistor
MET1…3	First, second, and third metal layer
MMIC	Monolithic microwave integrated circuit
PA	Power amplifier
RF	Radio frequency
TFR	Thin-film resistor
THz	Terahertz
UA	Unit amplifier
X2	Frequency doubler
X4	Frequency quadrupler

Executive Summary

This document reports on the development of the TIMES THz front-end circuits, which have been designed and fabricated utilizing Fraunhofer IAF's InGaAs-channel metamorphic high-electron-mobility transistor (mHEMT) technology with 35-nm gate length. To address the THz-frequency range from 250 to 325 GHz, frequency multiplier, mixer, and a multitude of amplifier circuits as well as fully integrated 300-GHz front-end circuits have been developed.

The circuit design, simulation results, as well as measurement data after on-wafer characterization are described in detail.

1. Introduction

1.1 Scope

This deliverable provides an overview on the THz circuit design, including the on-wafer measurement data before wafer dicing. The general scope is the description of the fabricated circuits, including crucial design considerations, and provide a summary of the measurement results in comparison to the targeted specifications.

1.2 Audience

This report is intended for public use.

1.3 Structure

The rest of the document is structured as follows:

- Section 2 provides a brief overview on the technology used for the circuit implementation.
- Section 3 gives a summary of the designed circuit design, including the measured on-wafer results.
- Section 4 presents the summary and conclusions.

Finally, additional information on the measurement setups is provided in the Appendix A.

2 35-nm InGaAs mHEMT Technology

The technology used in this project is Fraunhofer IAF's $In_{0.52}Al_{0.48}As/In_{0.8}Ga_{0.2}As$ mHEMT technology with 35-nm gate length. The metamorphic HEMT structure is grown by molecular beam epitaxy on 100-mm semi-insulating GaAs wafers. To adapt the lattice constant between the GaAs and the InAlAs/InGaAs double heterostructure, a metamorphic buffer with a linear $In_xAl_{0.48}Ga_{0.52-x}As$ (x = 0 → 0.52) transition is grown. The active devices are defined by a two-step electron beam lithography and are encapsulated in benzocyclobutene (BCB). A detailed description of the front-end-of-line process is given in [1]. This 35-nm mHEMT technology features a current-gain cutoff frequency f_T and power-gain cutoff frequency f_{max} above 500 GHz and 1000 GHz, respectively. The maximum transconductance is around 2500 mS/mm and the maximum drain current density is 1300 mA/mm with an off-state break down voltage above 3.5 V.

One of the key technology features, which determines in large part the implementation possibilities of compact integrated circuits, is the available layers in the back end of line (BEOL). The simplified cross section and available layers of the full-passivated BEOL is shown in Figure 1. The BEOL process includes 50-Ω/square NiCr thin film resistors (TFR) and an 80-nm-thick chemical vapor deposition (CVD) deposited SiN layer used for on-wafer metal-insulator-metal (MIM) capacitors. Three metal layers (MET1-MET3) are available for the design of compact matching networks with thin-film microstrip line (TFMSL) interconnects on the wafer front side. The electron-beam-evaporated Au-based first and second metal layers are defined in a lift-off process. MET3 is a 2.7-µm-thick plated Au layer, passivated by a BCB layer.
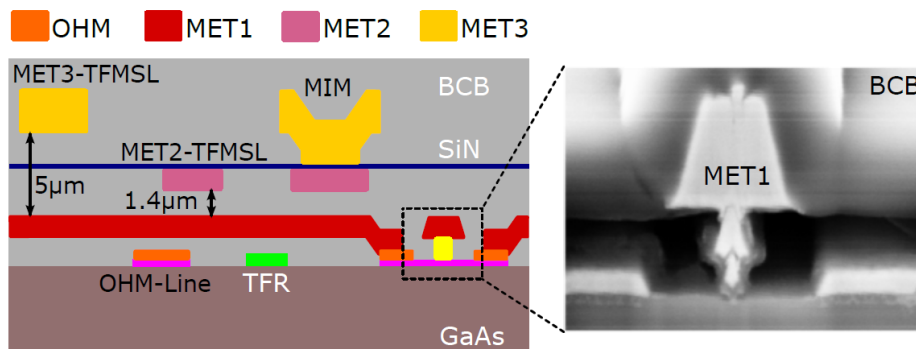

Figure 1: Schematic cross section (not to scale) of the three-metal-layer InGaAs mHEMT IC thin-film wiring environment on GaAs substrate. The available backside process including thru-substrate vias are not shown.

The most-important and typically-used types of transmission lines, which are relevant for the implementation of highly-compact THz circuits, are the TFMSLs illustrated in Figure 1. The first metal layer MET1 is typically used as RF shielding DC and RF ground and, consequently, MET3 and MET2 are primarily used for signal routing. For the routing of very low-current signals, the ohmic-layer on top of the epi stack as well as the TFR layer can also be used. The main advantage of using these layers is the possibility to route signals underneath the MET1 ground layer.

3 Circuit Design and Results

The topology of the THz front ends, which are operating in the frequency range around 300 GHz, are described in detail in the deliverable *D2.3 – Definition of scenarios and KPI for hardware demonstration and PoC* [2]. A simplified block diagram of the upconverter and downconverter is, additionally, depicted in Figure 2. To generate the LO signal for the RX and TX MMICs around 100 GHz, a frequency multiplier by four MMIC is used to multiply the input signal in the range between 10 to 30 GHz. The RX and TX MMICs include an additional multiplication stage, amplifier stages, as well as the mixer for the up and down conversion between the extended E-band IF frequency range and the targeted 250–325-GHz RF frequency band. In order to increase the available transmit power, additional high-power amplifier (HPA) circuits have been designed and fabricated.
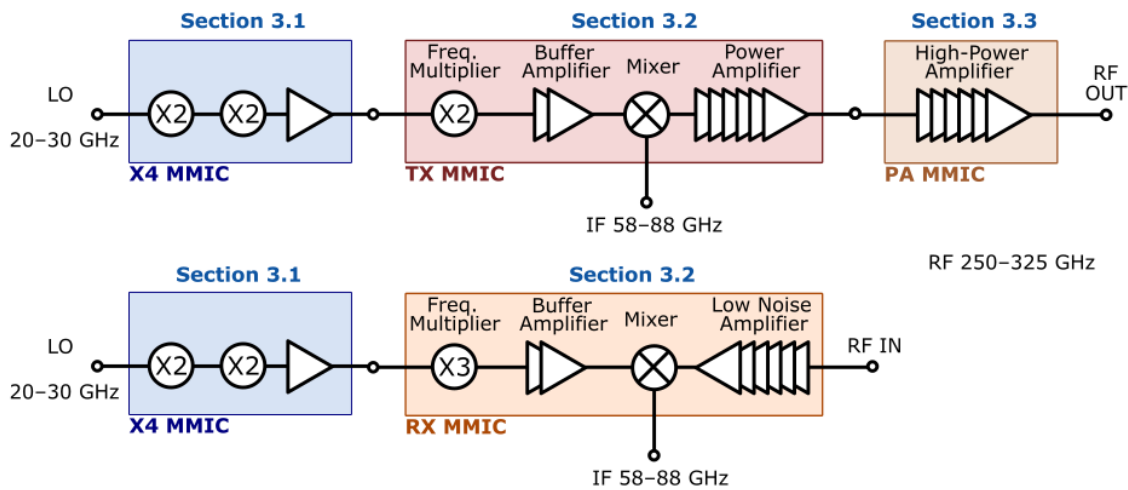

Figure 2: Simplified block diagram of the upconverter and downconverter with LO frequency around 25 GHz, E-band IF frequencies, and an RF frequency range between 250 to 325 GHz.

The circuits depicted in Figure 2, corresponding design considerations, as well as the measured on-wafer performance is described in the following subsections. The measurement setups are described in detail in Appendix A.

3.1 Frequency Multiplier by 4 MMIC

As shown in the block diagram in Figure 2, a frequency quadrupler (X4) is used to multiply the 25-GHz LO signal and to generate the LO input signal for the RX and TX MMICs described in the following sections.
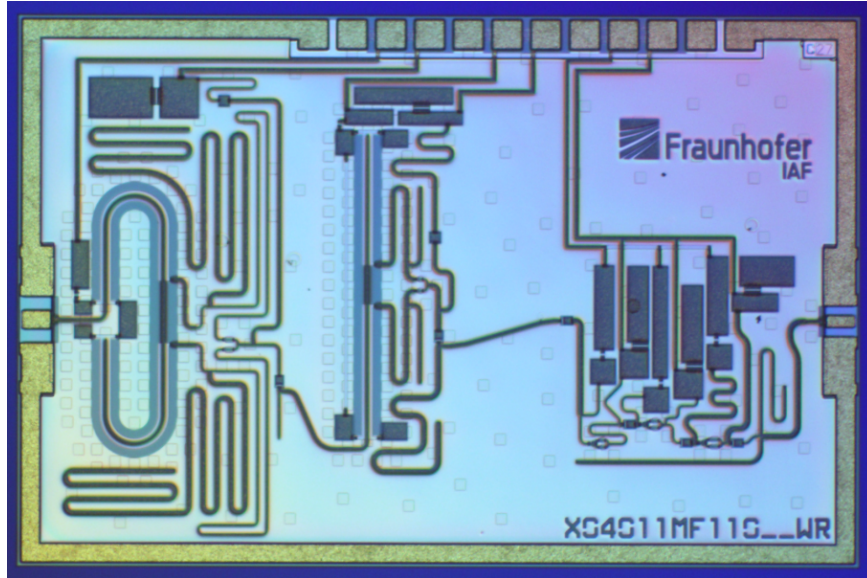

Figure 3: Chip photograph of a X4 MMIC. The chip dimensions are 2.25 x 1.5 mm².

Circuit Design The implemented circuit is shown with the chip photograph in Figure 3, utilizing a topology with two cascaded frequency-doubler stages, followed by a three-stage amplifier. The two doubler stages are implemented in a differential topology, which provides a very good suppression of unwanted uneven harmonics. To this end, each stage utilizes a vertically stacked Marchand balun to generate the differential input signal of the differential doubling stages as described in [3]. The amplifier at the output is used as an active filter and to increase the output power of the quadrupler circuit.

The simulated response of two X4 versions (X4_1 and X4_2) is shown in Figure 4. Depicted are the generated harmonics versus frequency (top) as well as a power sweep for both X4 circuits. The difference between the two circuits is the amplifier at the output stage, with X4_1 being designed for a slightly lower output frequency range as X4_2. According to the simulation, 5 to 8 dBm of output power are expected at the 4th harmonic between 90 to 140 GHz.

Measurement Results The measured saturated output power of the two X4 versions, plotted versus the output frequency of the 4th harmonic, are depicted in Figure 5. The measured power level of the 4th harmonic for X4_1 (on the left in Figure 5) is around 8 dBm between 85 to 110 GHz, showing a suppression of the unwanted harmonics in excess of 20 dB. At higher frequencies, however, the X4_1 circuit shows decreasing power levels of the 4th harmonic with substantially increasing power in the 5th harmonic. The X4_2, on the other hand, achieves with around 10 dBm of measured output power between 100 to 135 GHz a larger bandwidth while also achieving an improved suppression of the unwanted harmonics. The largest signal levels for the unwanted harmonics are measured for the 8th harmonic with power levels between -20 and -10 dBm. With these measured output power levels in the range of 8 to 10 dBm, sufficient LO power can be provided to the input of the RX and TX MMICs, which are described in the following sections.
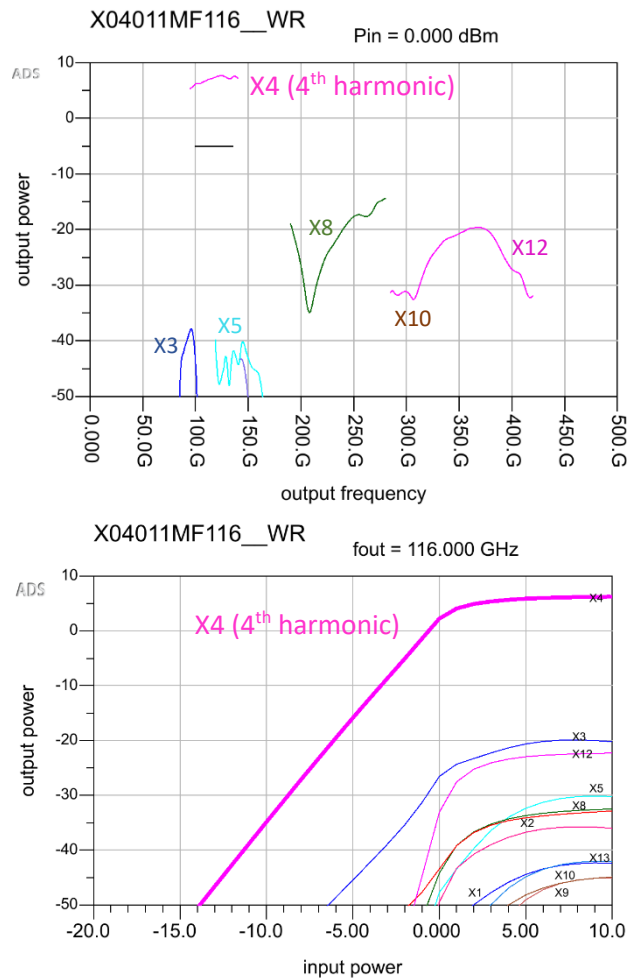
Multiplier X4_1
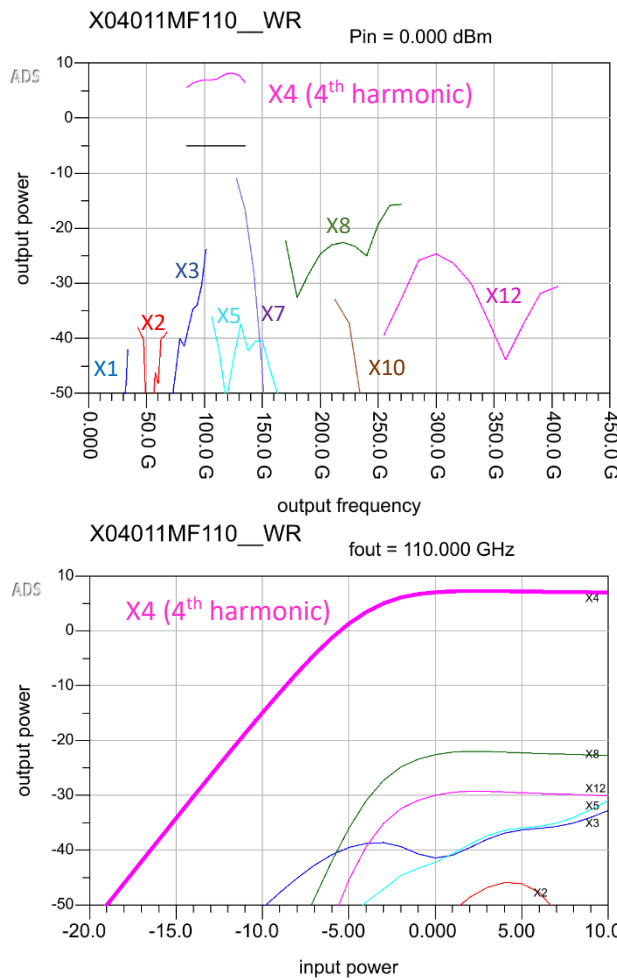
Multiplier X4_2

Figure 4: Simulated harmonics of the two frequency quadruplers. The upper plots show the generated harmonics versus frequency when applying an input frequency range around 22 to 32 GHz. The lower plots show the simulated output power in the different harmonic frequencies when sweeping the input power at 110 and 116 GHz, respectively. X1…12 labels the harmonic with the corresponding multiplication factor.
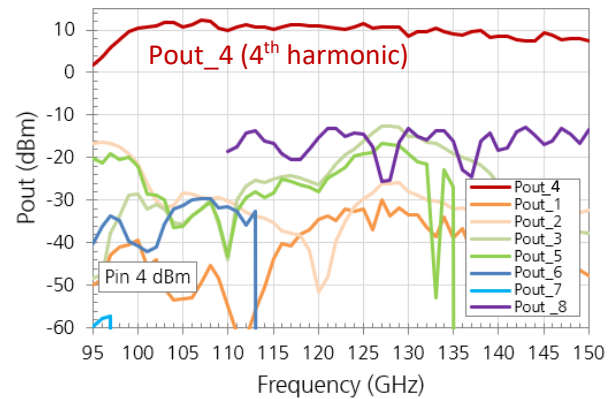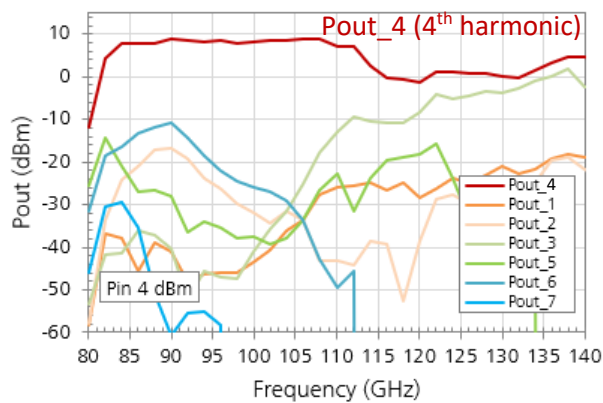

Figure 5: Measured output power of the different harmonics, plotted versus the output frequency of the 4th harmonic. At -4 dBm of input power, the frequency quadruplers are in saturation. Legend: Pout_1…8 describes the output power in the harmonic with the corresponding multiplication factor.

3.2   Transmit and Receive Front-End MMICs

The TX and RX MMICs are required for the up- and down-conversion of the 300-GHz RF signal from and to the extended E-band IF frequency range, using the 100-GHz LO signal which is generated by the above-described multiplier by 4 MMIC. The circuit implementation and the on-wafer measurement results are described in detail in the following subsections.

3.2.1   TX/RX LO-Chain

To drive the frontends' fundamental mixer, a frequency multiplier by two (X2) is needed in order to provide the required LO frequency range between 200 and 240 GHz which then converts the IF and RF signals between E-band (60-90 GHz) and H-band (250-325 GHz).
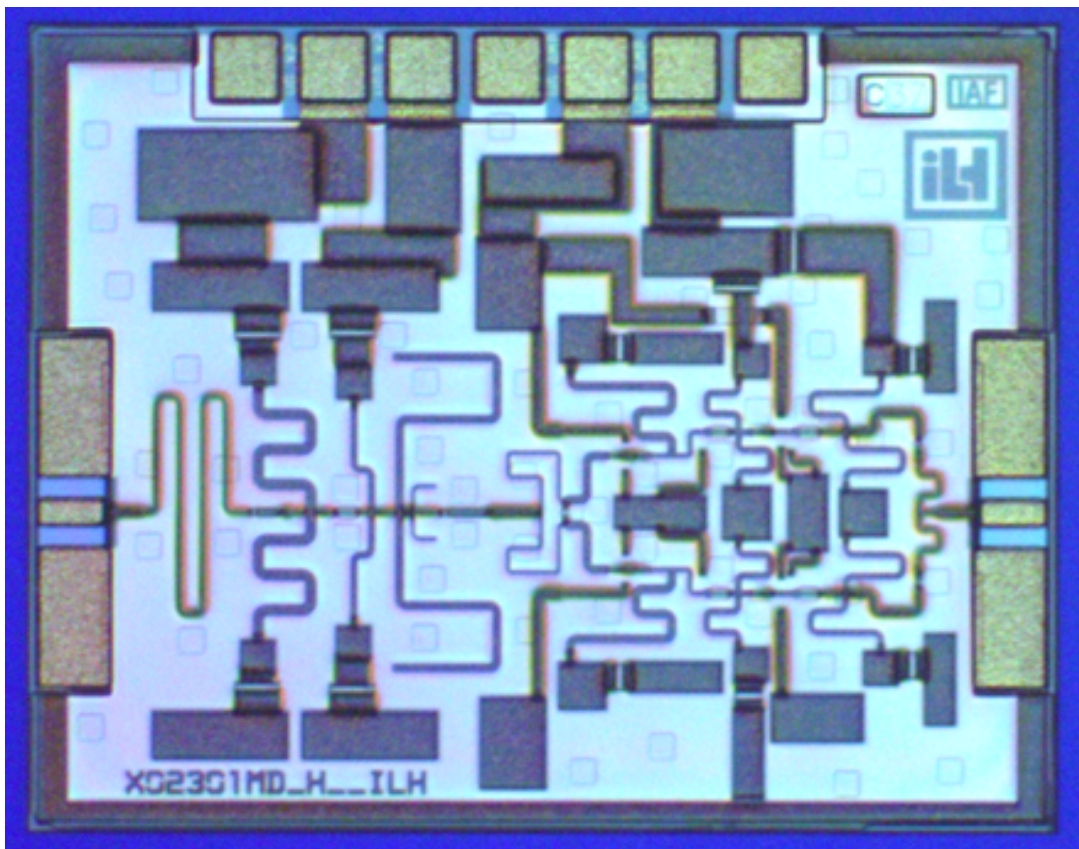

Figure 6: Chip photograph of the X2 break-out circuit, including the buffer amplifier at the output. The chip dimensions are 0.75 x 0.5 mm².

Circuit Design The frequency doubler is implemented utilizing a class-B operated common-source-HEMT. Using harmonic load-pull simulations, conversion gain and suppression of unwanted harmonics are optimized. To achieve the required LO drive power for the mixer, a buffer amplifier is added to the doubler output. The corresponding chip photograph of a break-out circuit including the X2 and the buffer amplifier is depicted in Figure 6.

The Buffer-amplifier consists of two stages, each with two parallel CS-HEMTs. It provides an additional amplification of 10 dB and a bandwidth form 200-240 GHz. In Figure 7, simulation results of the LO-chain are shown. While the simulated saturated output power is around 6.5 dBm, the minimum required output power

of 0 dBm is easily achieved, still leaving some margin. The simulations also predict a bandwidth from 92-122 GHz with respect to the input frequency, which is exceeds the required LO band of 100 to 120 GHz.

Measurement Results Initial on-wafer measurement results are shown in Figure 8, which prove the operability of the circuit. Overall, a slight shift of the performance towards higher frequencies is observed. The outstanding harmonic suppression of the third harmonic, which potentially is located in the RF frequency band of operation, is around -50 dBc for the measured frequencies. The output power tends to lower values compared to simulation but still the required 0 dBm are achieved for most frequencies.
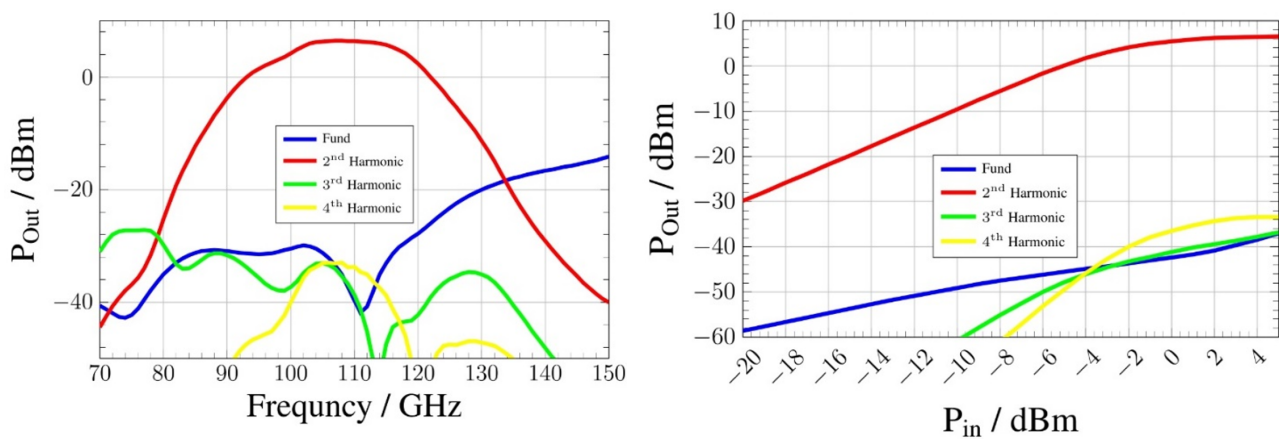

Figure 7: Simulation result of the X2 break-out circuit depicted in Figure 6: Simulated power of the harmonics versus the input frequency of the 2nd harmonic and power-sweep characteristic at 110 GHz.
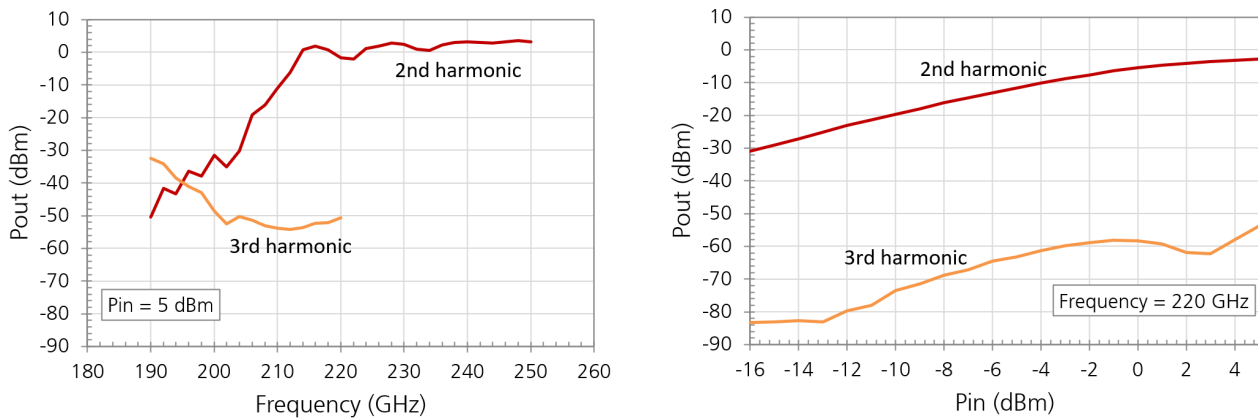

Figure 8: Measured output power of the 2nd and 3rd harmonics of the X2 break-out circuit.

3.2.2 Resistive Mixer

For the frequency conversion in both the Tx and Rx MMIC, a fundamental resistive mixer is used. It is designed for a LO-band of 200-240 GHz and requires a LO-power of 0 dBm. The IF band covers the E-band and the RF band covers the H-band.

Circuit Design The conversion gain of the resistive mixer is simulated to lie around -10 dB with an output referred 1dB-compression point of -13 dBm. Due to its reciprocal operation, the resistive mixer is used for TX and RX. Simulation results of the mixer including the LO-chain are shown in Figure 9 and Figure 10.

Figure 9 shows the simulation results for the TX operation. The output power over the RF-frequency is shown for an IF power of -10 dBm. The simulations show that using a LO band from 100-120 GHz are sufficient for covering the 250 to 325-GHz frequency range. Also, an IF power sweep is shown, which show a good linearity, which is expected for a passive mixer like the used resistive. Figure 10 shows the RX operation simulation results. In the first plot, the conversion gain (CG) plotted over the RF frequency is shown. There it can be seen, that also for the RX operation the 260 to 330-GHz frequency band can be covered using the resistive mixer. The right plot shows a power sweep over RF power, which shows a slightly lower linearity compared to the TX operation but still in a good operation region. No breakout circuit for the mixer circuit was fabricated and measured.
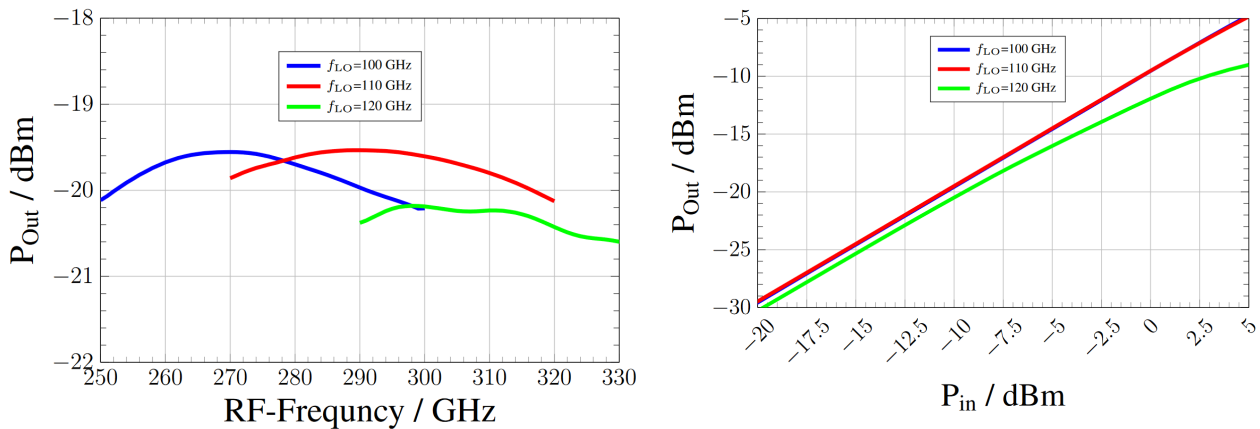

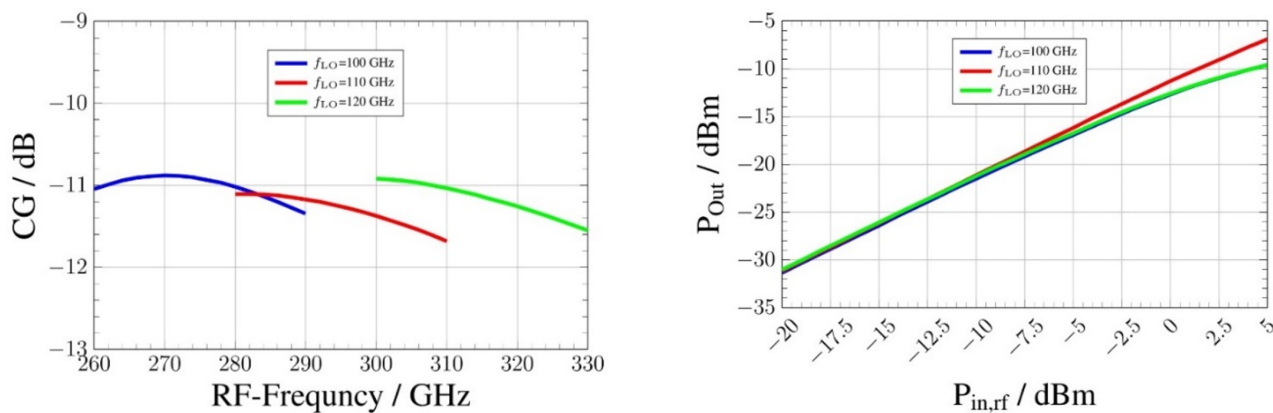*Figure 9: Simulation results of the resistive mixer including the on-chip LO-chain for the TX case.*

Figure 10: Simulation result of the resistive mixer including the on-chip LO-chain (left) conversion gain versus RF frequency for an LO power of 3 dBm and a RF power of -10 dBm and (right) output power sweep versus RF power for an LO power of 3 dBm.

3.2.3 RF Power Amplifier

To perform on-chip RF-signal amplification of the previously described resistive mixer in the TX as well as the RX MMIC, a seven-stage power amplifier is implemented.

Circuit Design The chip photograph of a break-out circuit containing the RF power amplifier is depicted in Figure 11. While the first three stages use single common-source transistor devices with a unit gate width of 10 um and source degeneration to operate as low-noise amplifier, the following four stages use standard common-source devices and parallelization to increase the achievable output power. Stages four and five use two parallel two-finger common-source (CS) devices and the stages six and seven use four parallel devices, all with the same unit-gate width of 16 um.
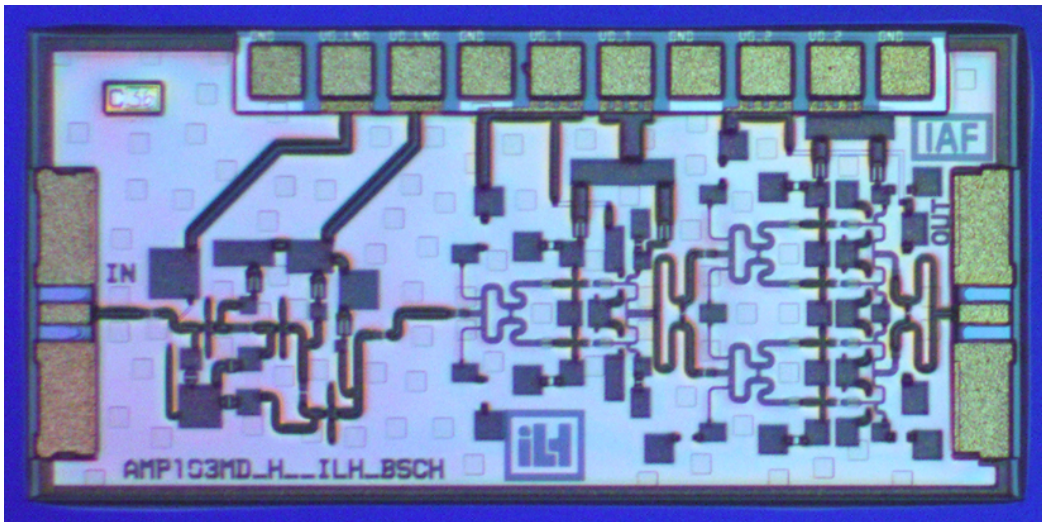

Figure 11: Chip photograph of the RF power amplifier break-out circuit. The chip dimensions are 1.5 x 0.75 mm².

The simulated S-parameters as well as large-signal behaviour of the RF power amplifier are depicted in Figure 12. The expected small-signal gain is around 30 dB with a small signal bandwidth spanning from 240 to 320 GHz. The simulated saturated output power is 10 dBm at 300 GHz with a 1-dB compression point around 4 dBm.

Measurement Results The initial on-wafer measured S-parameter performance of the 7-stage RF LNA/PA is shown in Figure 13, proving the operability of the amplifier in the frequency range of around 270 to 325 GHz. Depicted are the measurement results for different bias conditions in order to verify the gain levels that can be achieved at different bias settings and to illustrate the impact of the measurement setup. Due to the high gain of the amplifier of up to 35 dB and the limited isolation in the on-wafer measurement setup (coupling between the RF probes), the gain as well as the matching show a significant ripple for larger current densities and thus larger gain values. This is very typical for on-wafer measured gain values larger than 20 dB (e.g. see [4]). The bandwidth limitations at the lower band edge need to be further investigated in simulation.

On-wafer measurements of gain versus output power show an achievable saturated output power up to 6 dBm with output related 1-dB compression points around 0 dBm. At very low gain levels, a good linear behaviour is still observed. Hence, the gain of the amplifier, implemented in the RX and TX circuits, can be optimized for the application scenario required in WP6.
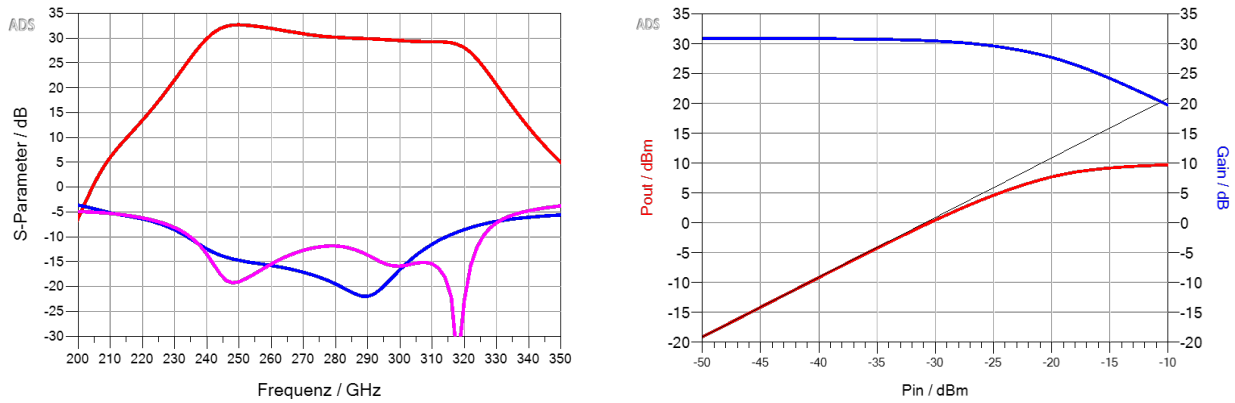
Figure 12: Simulated S-parameters (left) and simulated large-signal characteristics (right) of the RF power amplifier.
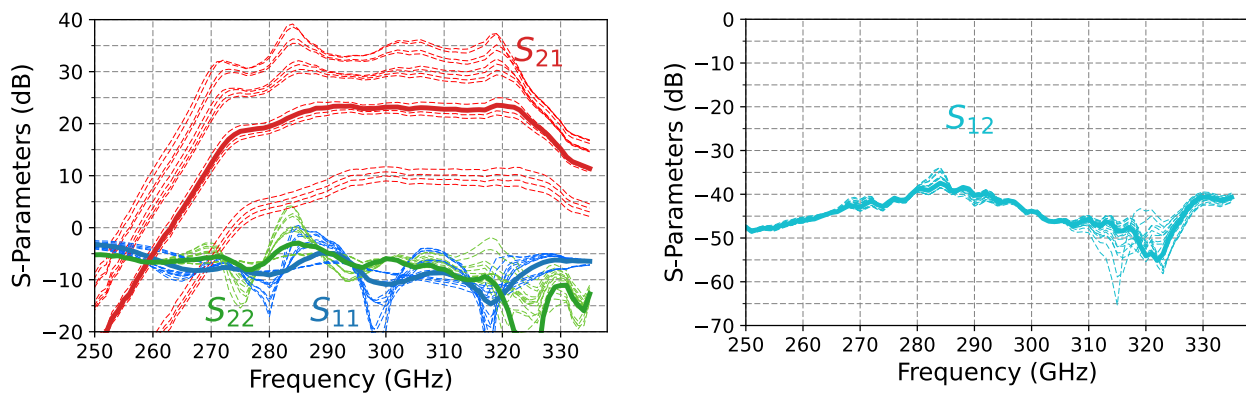

Figure 13: Measured S-parameters of the 300-GHz PA circuit. The measured S11, S21, and S22 parameters are shown on the right. The measured S12, which is limited by the coupling between the RF probes, is shown on the right. Depicted is the on-wafer data for different bias conditions. The drain voltage was varied between 0.9 and 1.2 V in 100-mV step size and the drain current was swept from 50 to 200 mA/mm in 50-mA/mm step size. Highlighted with the solid line is the bias condition with 100 mA/mm and 1.1 V.
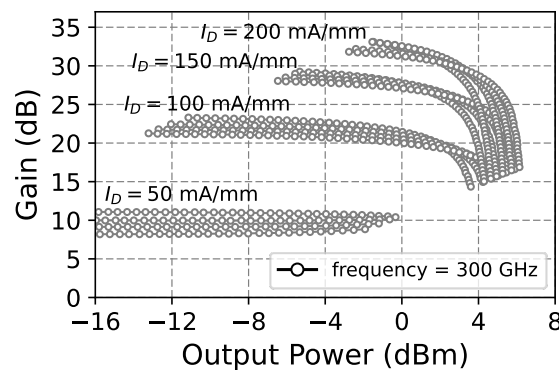

Figure 14: On-wafer measured gain versus output-power characteristics of the 300-GHz PA circuit. Depicted is the data for drain currents between 50 and 200 mA/mm and drain-voltage values between 0.9 and 1.2 V.

3.2.4   RX MMIC

The RX MMIC will be used for the down conversion of the 300-GHz RF signal to the extended E-band IF frequency range, using the 110-GHz LO signal which is generated by the above-described multiplier by 4 MMIC (Section 3.1). The circuit implementation and the on-wafer measurement results for the RX MMIC are described in detail in the following subsections.
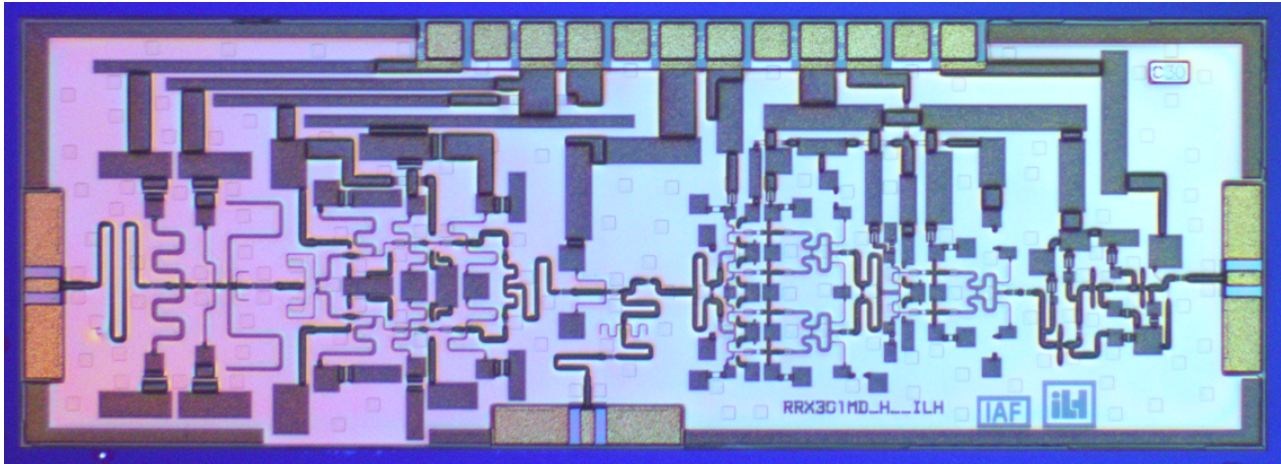

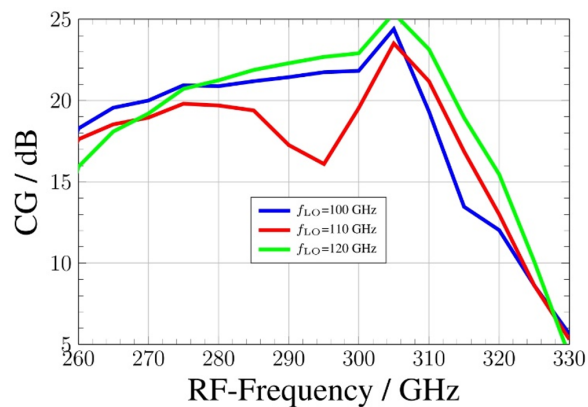Figure 15: Chip photograph of the RX circuit. The chip dimensions are 2.75 x 1.0 mm².

Figure 16: Simulated conversion gain of the full-integrated RX circuit depicted in Figure 15.

Circuit Design The receiver is designed to implement a super-heterodyne architecture. To this end, the modulated baseband data is provided on an intermediate frequency, which is located in the E-band spanning from 60 to 90 GHz. The targeted RX RF frequency is operating in H-band between 250 and 325 GHz. Hence, the required LO frequency range for the conversion between E- and H-band is around 100 – 120 GHz. The corresponding block diagram of the RX frontend is depicted in Figure 1, implementing the LO chain described in Section 3.2.1 as well as the fundamental resistive mixer and the RF power amplifier described in sections 3.2.2 and 3.2.3. The chip photograph of the fully-integrated RX MMIC is depicted in Figure 15.

Simulation results for the RX circuit are shown in Figure 16, predicting an operable RF bandwidth of around 260 to 310 GHz. There the CG plotted over the RF-frequency is around 20 dB with dependencies on the used combination of RF and LO frequencies.

Measurement Data Initial on-wafer measurement results pare shown in Figure 17 to Figure 18. Overall, an operational RF bandwidth of 275 to 325 GHz is achieved. The IF interface is measured so far to be able to

handle frequencies between 70 and 90 GHz. Further measurements will specify the bandwidth in more detail. Furthermore, the LO tuning proves to work within a frequency range of 95 and 125 GHz and the RF input power sweep conducted at 300 GHz reveals an input-related 1-dB compression point of around -25 dBm of RF input power as shown in Figure 18.
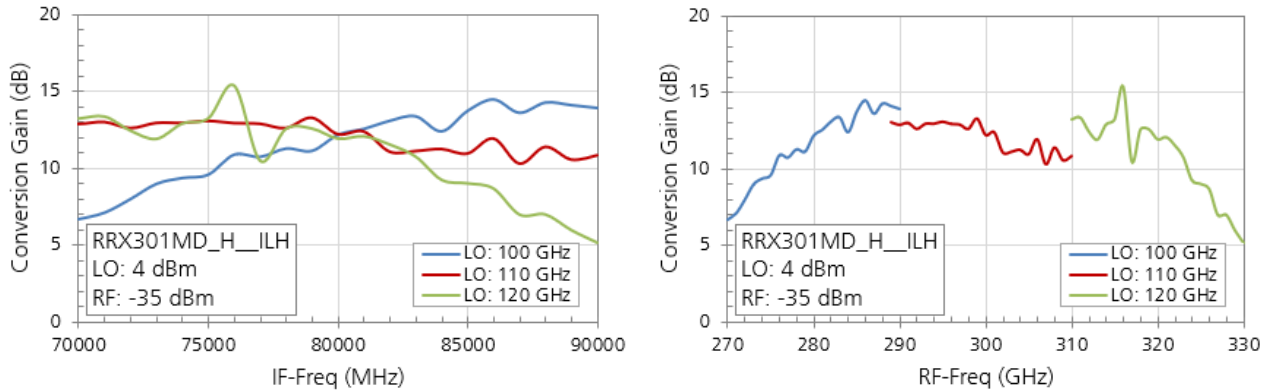

Figure 17: CW measured CG of the RX circuit for LO frequencies between 100 to 120 GHz. Depicted is the CG versus the IF frequency range of 70 to 90 GHz on the left and versus the corresponding RF frequencies on the right.
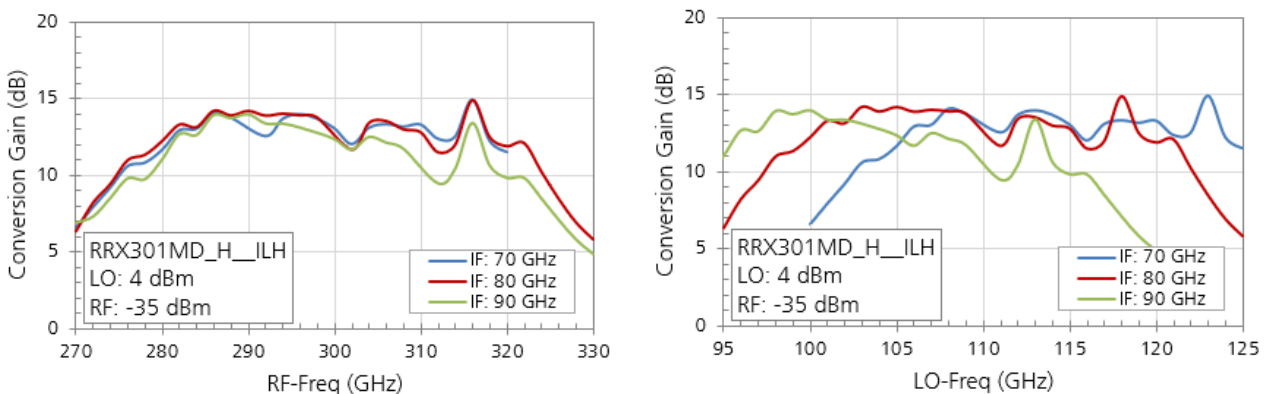

Figure 18: Measured CG for IF frequencies of 70 GHz, 80 GHz, and 90 GHz. Depicted is the CG versus the RF frequency range of 270 to 330 GHz and versus the corresponding LO frequencies between 95 and 125 GHz
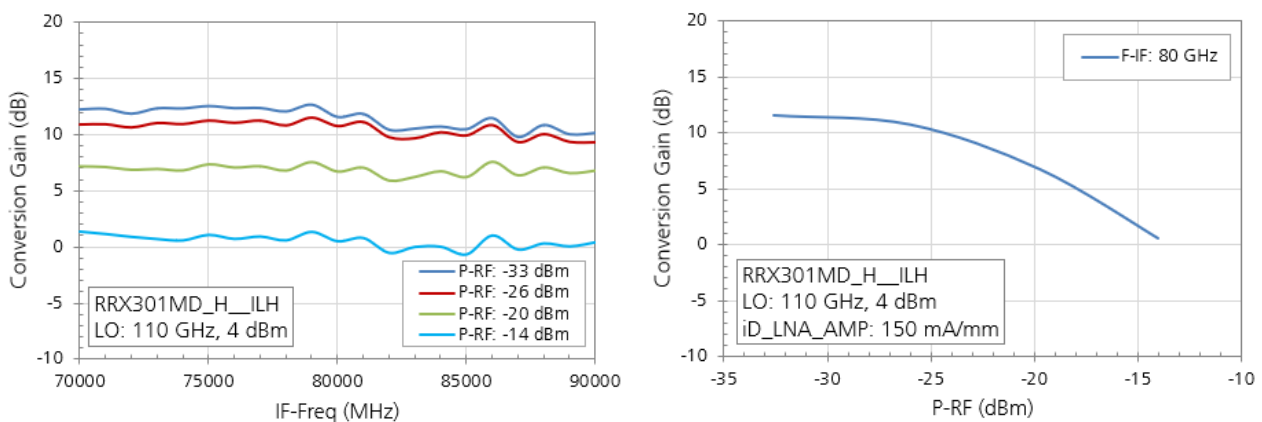

Figure 19: Measured CG for different RF-input-power levels. Depicted on the right is the CG versus the IF frequency for power levels between -33 and -14 dBm. The right plot shows the gain-compression characteristics.

3.2.5   TX MMIC

The TX MMIC is required for the up conversion of the E-Band IF signals to the targeted 250–325-GHz RF frequency band, using the 110-GHz LO signal which is generated by the above-described multiplier by 4 MMIC (Section 3.1). The circuit implementation and the on-wafer measurement results are described in detail in the following subsections.
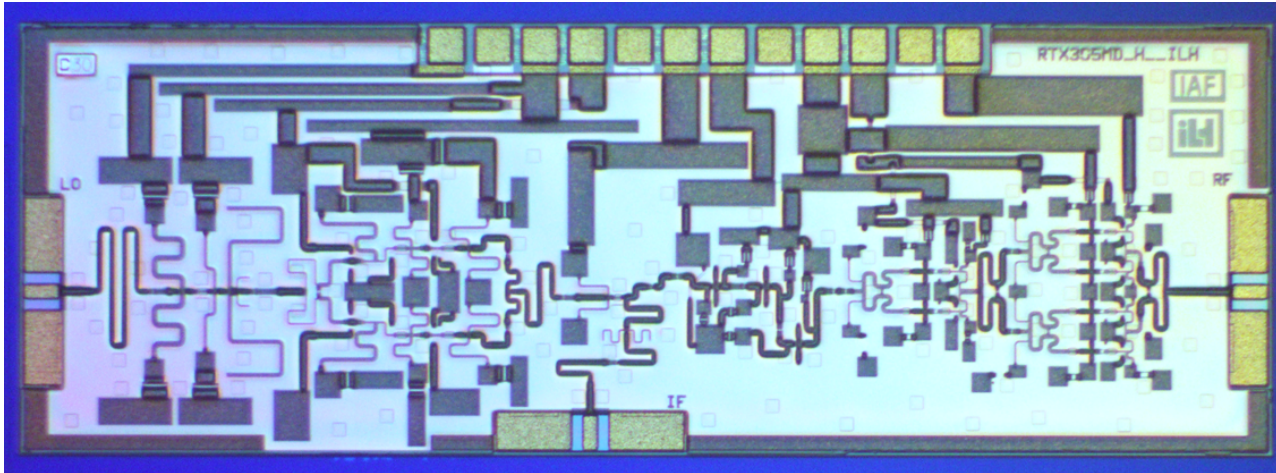

Figure 20: Chip photograph of the TX circuit. The chip dimensions are 2.75 x 1.0 mm².

Circuit Design As described in the above sections, the TX implements the same LO-chain and mixer for the frequency conversion as the RX. Therefore, the results presented in the previous chapters are still applicable here. For the amplification and to provide the required RF output power for long distance transmission the same 7 stage amplifier as for the RX is used. Due to the stages a high gain of over 30 dB can be achieved and the last stage is optimized for high power of up to 8 dBm without any additional subsequent HPA stage. A block diagram of the TX was introduced in Figure 2. The corresponding chip photograph of the fully-integrated TX circuit is shown in Figure 20.

Simulation results of the achievable RF output power versus RF frequency are shown for different LO frequencies in **Error! Reference source not found.**. Here the overall bandwidth can be seen, which is around 50 GHz. It can be seen, that for a LO frequency of 120 GHz the overall gain is about 5 dB lower compared to the other simulations. This is due to the LO feed through, which lies close to the operation band of the amplifier and therefore starts driving it into compression. This can also be seen in the second figure, were the output power over the LO power is shown.

Measurement Data Initial on-wafer measurement results are shown in Figure 22 to Figure 25 and prove the operability of the transmitter circuit. As for the previously described circuits, the TX as well shows a slightly shifted performance to higher frequencies. An operational RF bandwidth of 55 GHz between 270 to 325 GHz has been achieved. The IF bandwidth extends as measured so far at least from 70 to 90 GHz. Further measurements will specify the performance in more detail.
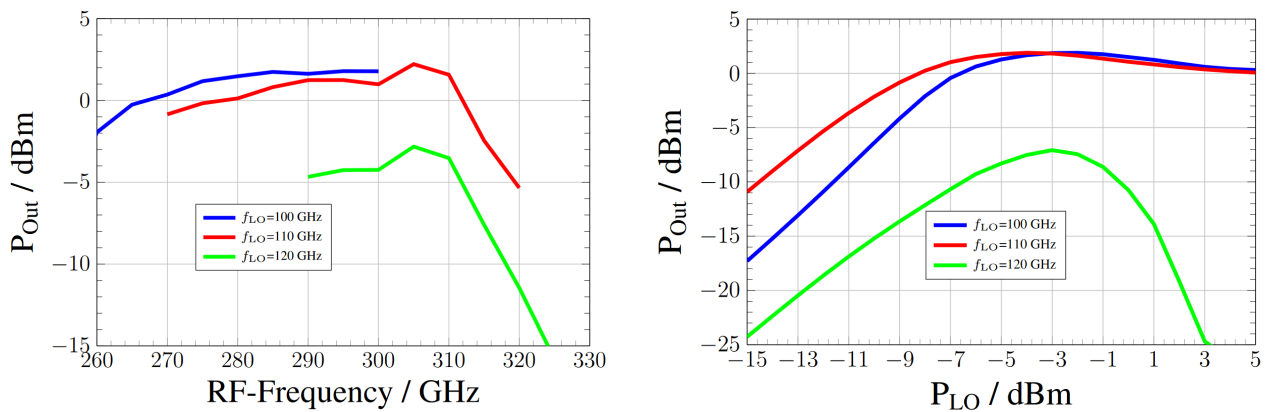
Figure 21: Simulation results of the resistive mixer including the on-chip LO-chain: (left) conversion gain over RF frequency for an LO power of 3 dBm and a RF power of -10 dBm, and (right) output power swept over RF power for an LO power of 3 dBm.
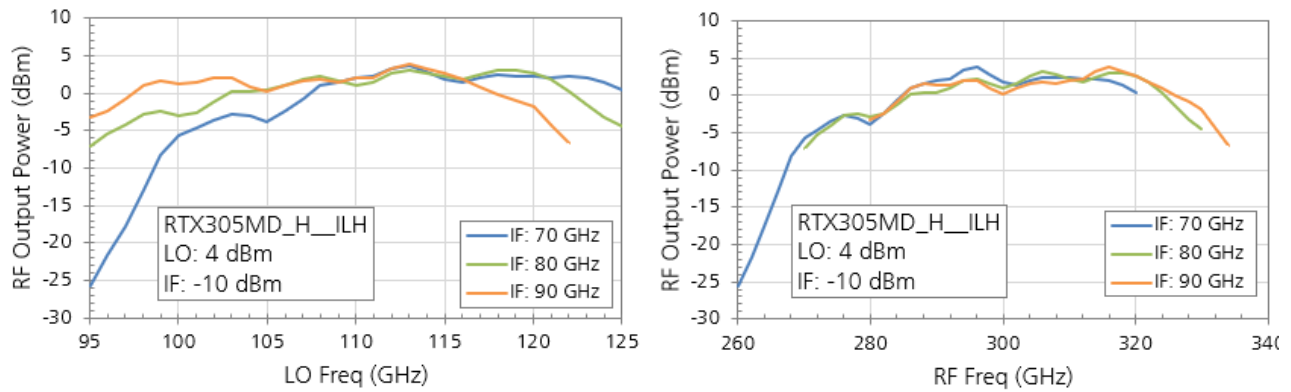

Figure 22: Measured RF output power of the TX circuit for IF frequencies at 70 GHz, 80 GHz, and 90 GHz. Depicted is the data versus the LO frequency on the left and versus the corresponding RF frequency on the right.
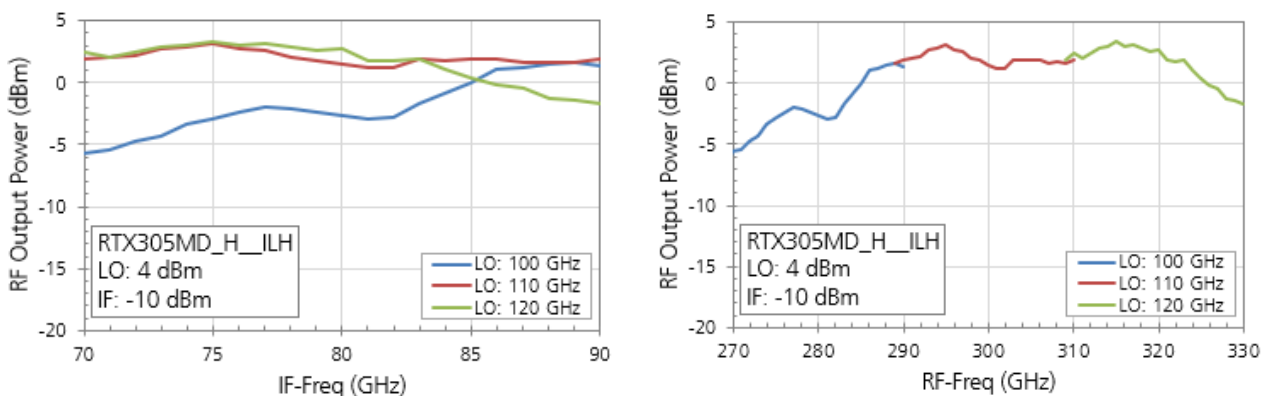

Figure 23: Measured RF output power of the TX circuit for LO frequencies of 100 GHz, 110 GHz, and 120 GHz. Depicted is the data versus the IF frequency on the left and versus the corresponding RF frequency on the right.
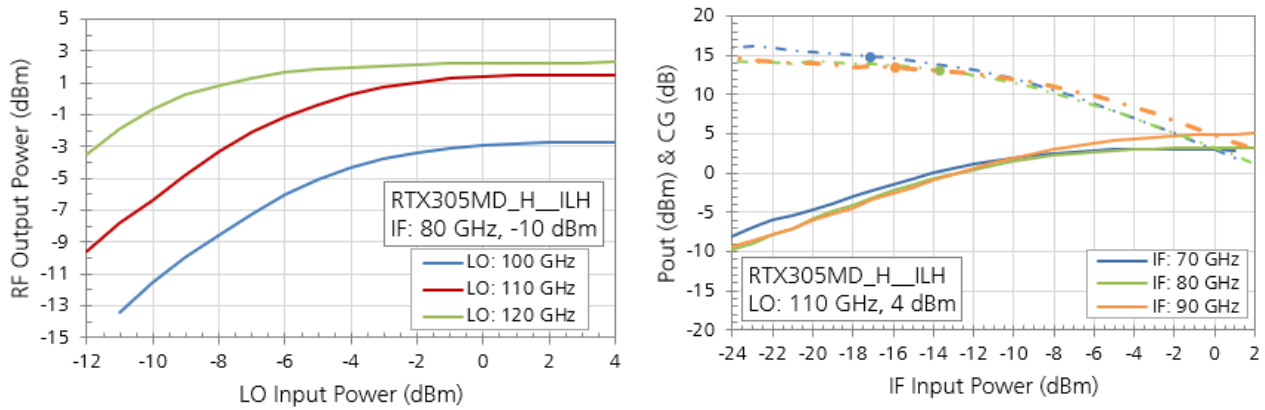
Figure 24: Measured RF output power versus LO input power (left) and IF input power (right).
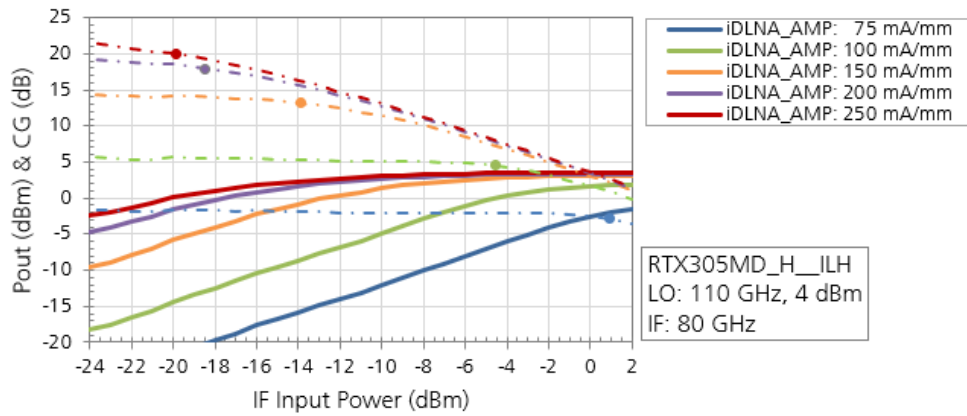

Figure 25: Measured RF output power and conversion gain versus the IF input power for different bias conditions of the RF amplifier. The drain current was swept from 75 to 250 mA/mm. The 1-dB compression point is highlighted with the round marker on the conversion-gain corves.

3.3 High-Power Amplifier MMICs

The HPA MMICs will be used to increase the available transmit power in the targeted RF frequency band around 300 GHz. The circuit implementation and the on-wafer measurement results are described in detail in the following subsections.

Circuit Design The PA circuits that have been developed for the TIMES front ends are based on a super-compact unit-amplifier (UA) cell, which can easily be placed several times in parallel [5]. In total, two PA variants have been fabricated: a 2-way-combined PA circuit and a 4-way-combined PA circuit. The chip photographs of these three circuit variants are depicted in Figure 26.

2-way combined-PA, chip size: 1.25 x 0.4 mm²
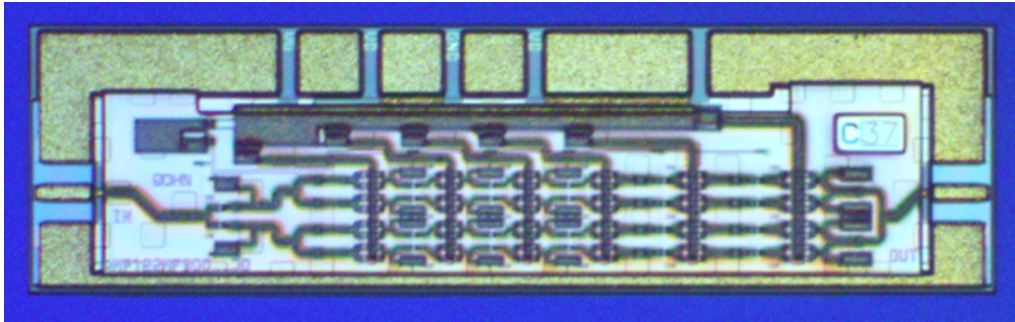
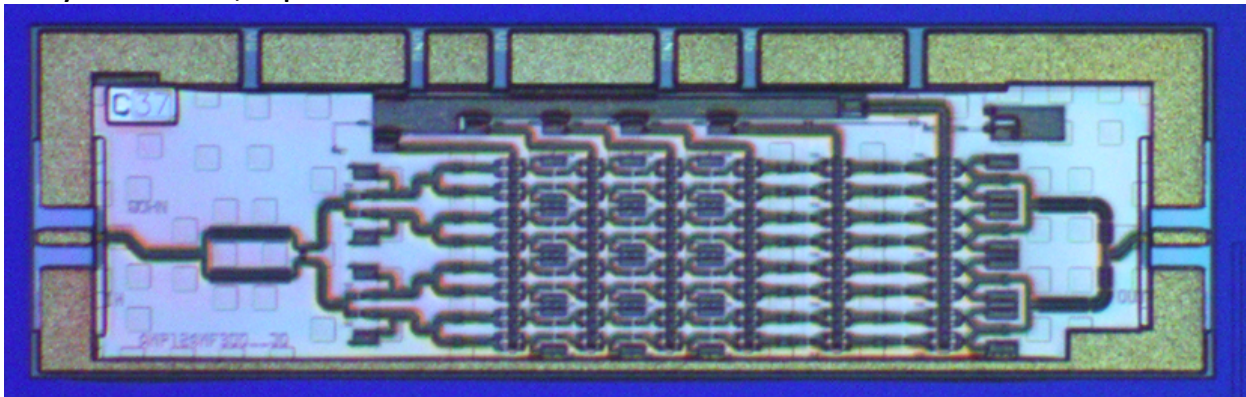**4-way-combined PA, chip size: 1.5 x 0.5 mm²**

*Figure 26: **Chip photographs of the** fabricated 2-way- and 4-way-combined PA circuits.*
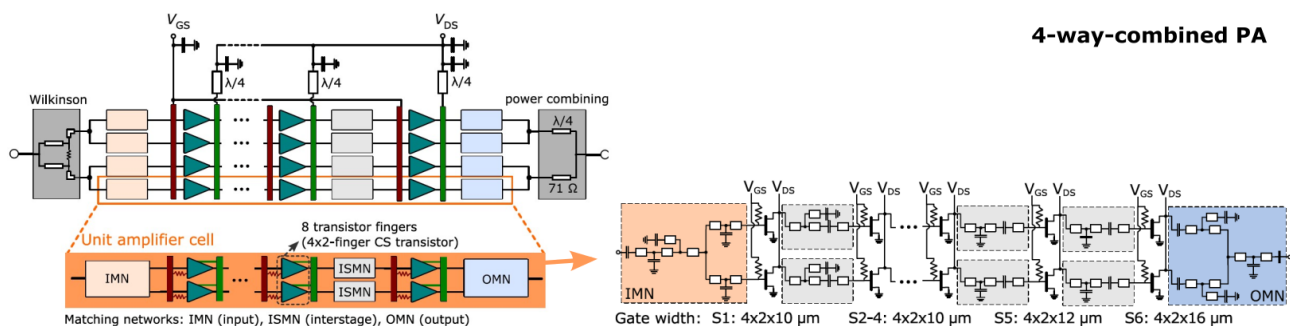

Figure 27: Block diagram of the 4-way-combined PA MMIC including a simplified schematic of the unit-amplifier cell that is placed in parallel four times.

The UA cell is matched to a reference impedance of 100 Ohm. This is done to allow the straight-forward parallelization of two UA cells by simply connecting their input and output nodes, which can be seen in the 2-way-combined PA circuit in Figure 26: Chip photographs of the fabricated 2-way- and 4-way-combined PA circuits. Based on this 2-way-combined 50-Ohm PA cell, the 4-way-combined PA circuit is implemented by using 50-Ohm power dividers and combiners at the input and the output, respectively. As an example, Figure 27 shows the simplified block diagram of the 4-way-combined PA circuit, including a circuit diagram of the UA cell. At the input, a Wilkinson power divider is utilized for the power splitting. In contrast, the power combining at the output is simply implemented by using high-impedance quarter-wave-length transmission lines as described in [5].

To achieve the super compact chip dimensions of the implemented UA, a novel bias-insertion concept was introduced and reported in [5], which allows the complete separation between the bias-distribution across a large number of parallel transistors and the matching between the cascaded gain stages. For the vertical distribution of the gate voltages, the OHM-Line and TFR layer depicted in Figure 1 are used, which allow the routing underneath the MET1 ground layer, completely independent from the matching networks.

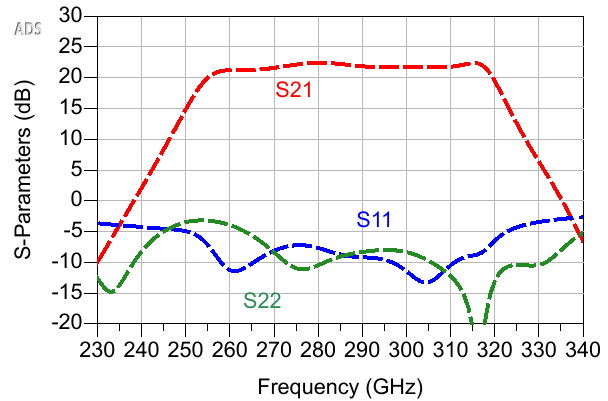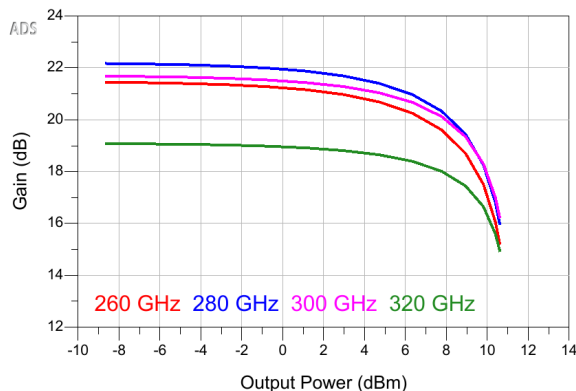**2-way combined-PA**
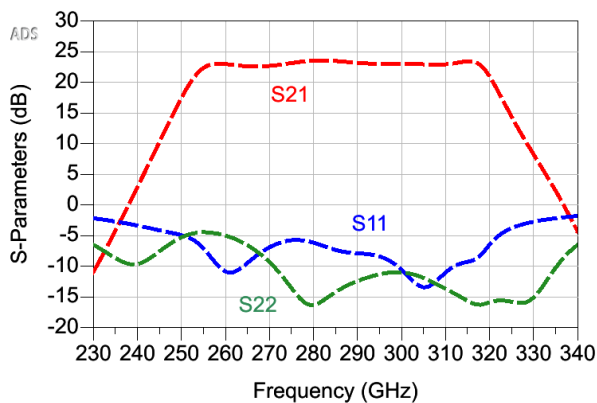
4-way combined-PA

Figure 28: Simulated S-parameters of the 2-way- (left) and 4-way-combined (right) PA circuits.

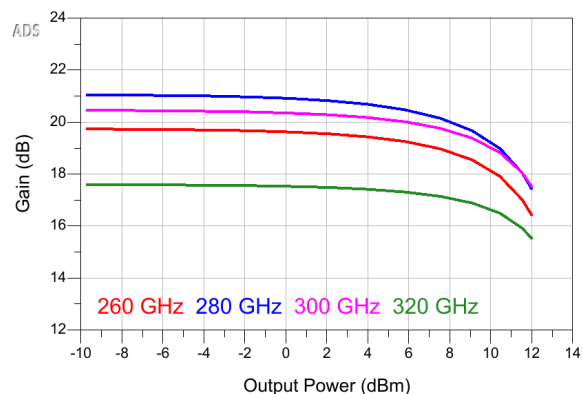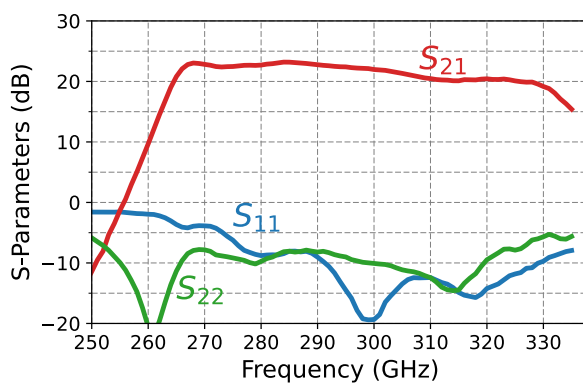**2-way combined-PA**

4-way combined-PA

Figure 29: simulated large-signal response of the 2-way- and 4-way-combined PA circuits, showing the compression behaviour with the gain plotted versus the output power characteristics.

The simulated S-parameters of the 2-way- and the 4-way-combined PAs are depicted in Figure 28. A flat gain response in the range slightly above 20 dB is expected according to the simulation between 255 and 320 GHz. The power splitting and combining in the 4-way design only shows a slight impact on the gain with around 1.5 to 2 dB total losses. The simulated large-signal characteristic for both PAs are shown in Figure 29, depicting the simulated gain versus output power characteristics. For the 2-way design, a maximum output power in the range of 10 dBm is expected, featuring a output-related 1-dB compression point of appr. 6 dBm at 300 GHz. For the 4-way design, up to 12 dBm saturated output power is expected.

Measurement Results The on-wafer measured amplifier results for the 2-way and the 4-way design are summarized in Figure 30 to Figure 32. Figure 30 shows the measured S-parameters for both amplifiers. The 2-way design achieves a small-signal bandwidth in excess of 60 GHz, from appr. 265 to 330 GHz. Hence, showing a shift to higher frequencies of around 10 GHz in comparison to the simulation. The 4-way combined design has a slightly lower upper band edge between 310 and 320 GHz, which was not expected based on the Simulation. This lower band edge in comparison to the 2-way design will be caused by the power splitting at the input or the power combining at the output.

The measured large-signal results for both amplifiers are shown in Figure 31 and Figure 32. Depicted are the measured gain and output power versus the input power on the left and the compression characteristics with the measured gain versus measured output power in the plot on the right. Since the power measurements were done with the waveguide extension modules used in the S-parameter setup, the input power was limited to power levels below -10 dBm. Therefore, the amplifiers were not measured into deep gain compression. The 2-way design achieves the targeted 1-dB compression (OP1dB) point at output power levels slightly above 6 dBm and an expected saturated output power around 10 dBm. In addition, for the 4-way design, the expected OP1dB of 8 dBm was achieved. These measurements are performed at a relayed bias condition at 1 V drain source voltage.

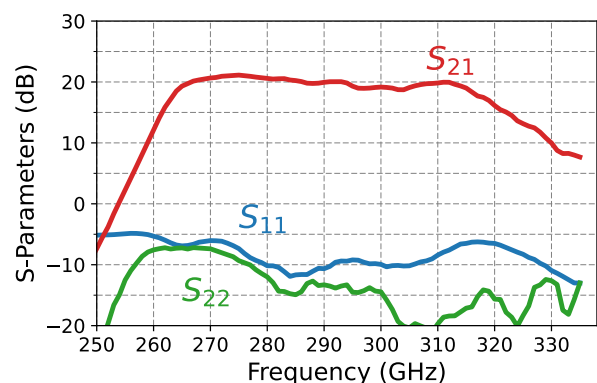**2-way combined-PA**

4-way combined-PA

Figure 30: On-wafer measured S-parameters of the 2-way- and 4-way-combined PA circuits.

2-way combined-PA

Figure 31: Measured on-wafer large-signal characteristic of the 2-way-combined PA at 300 GHz. Depicted are the large-signal gain and output power versus the input power (left) and the gain-compression characteristic can be seen with the gain plotted versus the output power on the right.
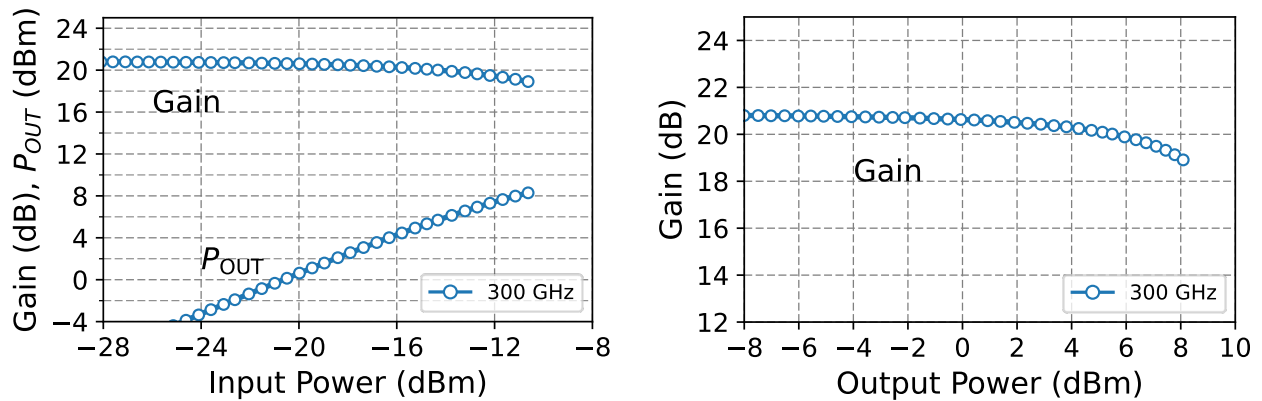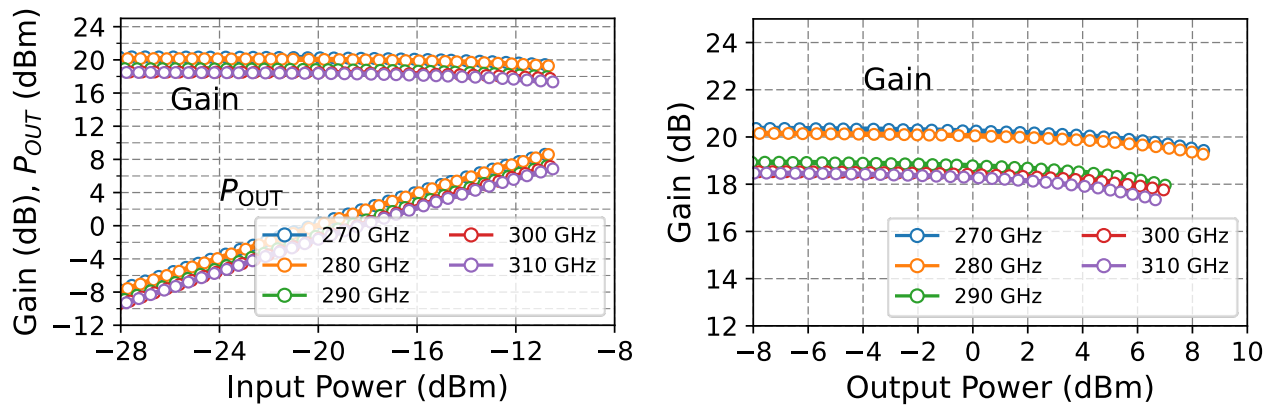
4-way combined-PA

Figure 32: Measured on-wafer large-signal characteristic of the 4-way-combined PA between 270 and 310 GHz. Depicted are the large-signal gain and output power versus the input power (left) and the gain-compression characteristic can be seen with the gain plotted versus the output power on the right.

4   Conclusions

The first generation of 300-GHz front-end circuits for the TIMES PoC have been fabricated and initially characterized. All circuits are operational and show a slight frequency shift to higher frequencies, which needs to be expected due to the impact of minor process variations at these high frequency bands. In the following, these circuit results for the TIMES THz front ends are summarized in comparison to the targeted values which have been initially described in [2] "D2.3 – Definition of scenarios and KPI for hardware" in the beginning of the project.

Electrical specifications TX FE	Target Values	Measured Values
RF frequency range (GHz)	250 – 325	270 – 325
RF output power (including HPA) (dBm, OP1dB)	> 6	> 6
IF frequency range (GHz)	58 – 90	70^1 – 90
IF input power (dBm, IP1dB)	−5 … 0	−15 … -5^2
IF input power (dBm, damage)	5 … 10	5 … 10

1) The IF frequency range was limited by the measurement setup to E-band frequencies between 60 to 90 GHz.
2) The IP1dB depends on the gain of the RF power amplifier, which can be tuned over a range of 20 dB.

Electrical specifications RX FE	Target Values	Measured Values
RF frequency range (GHz)	250 – 325	270 – 325
RF input power (dBm, IP1dB)	−30 … −20	−25
RF input power (dBm, damage)	− 15	− 15
IF frequency range (GHz)	58 – 90	70^1 – 90
IF output power (dBm, OP1dB)	−18 … −13	− 15

1) The IF frequency range was limited by the measurement setup to E-band frequencies between 60 to 90 GHz.

Overall, the measured performance of the front-end circuits is in good agreement with the target values. The main deviation is the bandwidth limitation to the frequency range above 270 GHz, which is addressed in a redesign of the THz circuits that will be fabricated and available in early 2025 and could be implemented in a later version of the front-end modules. Since the measurement setups for the initial characterization were limited to IF frequencies at E-band, the performance verification for 60-GHz IF frequencies is still pending. Based on the results reported in this document, however, it is expected that IF frequencies below 70 GHz can be used in conjunction with LO frequencies above 110 GHz without any issues.

Based on the successful verification of the MMIC performance, the module design will proceed in T5.2 and the PoC planning can be further narrowed down in WP6.

5   References

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[2] TIMES, "D2.3 - Definition of scenarios and KPI for hardware," 2023.

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[5] L. John, S. Wagner, A. Tessmann and A. Leuther, "Highly-Compact 20-mW, 270–320-GHz InGaAs mHEMT Power Amplifier MMIC," in *IEEE MTT-S International Microwave Symposium (IMS)*, Washington DC, 2024.

6 Appendix A – Measurement Setups

For the initial on-wafer characterization different setups were used.

- The WR-3.4 on-wafer S-parameter characterization was done using a Keysight N5224B PNA system and Virginia Diodes, Inc. (VDI) extension modules. The entire setup was calibrated to the probe tip of the RF probes by performing a thru-reflect-line calibration, using an impedance standard substrate (ISS).
  Additional power measurements of the amplifier circuits were performed using this setup.
- Scalar power measurement of the multiplier by 4 MMICs were done using a Keysight E8257D signal generator and an Anritsu MS2760A Spectrum Analyzer.
- Scalar power measurements of the X2 and the LO chain were performed using a Keysight E8257D signal generator in conjunction with different commercial and custom-built frequency multipliers at the input and a Keysight N9030A PXA Signal Analyzer with external mixer at the output.
- The LO and IF signals for the TX characterization were generated using a Keysight E8257D signal generator and a Keysight 83650A Synthesized Sweeper in conjunction with multiplier modules. At the RF output, a Keysight N9030A PXA Signal Analyzer with external mixer was used.
- For the RX characterization, the WR3.4 RF signal was generated using a Keysight 83650A signal sweeper and for the LO signal a Keysight E8257D signal generator. The down converted IF signal was measured using an Anritsu MS2760A Spectrum Analyzer.